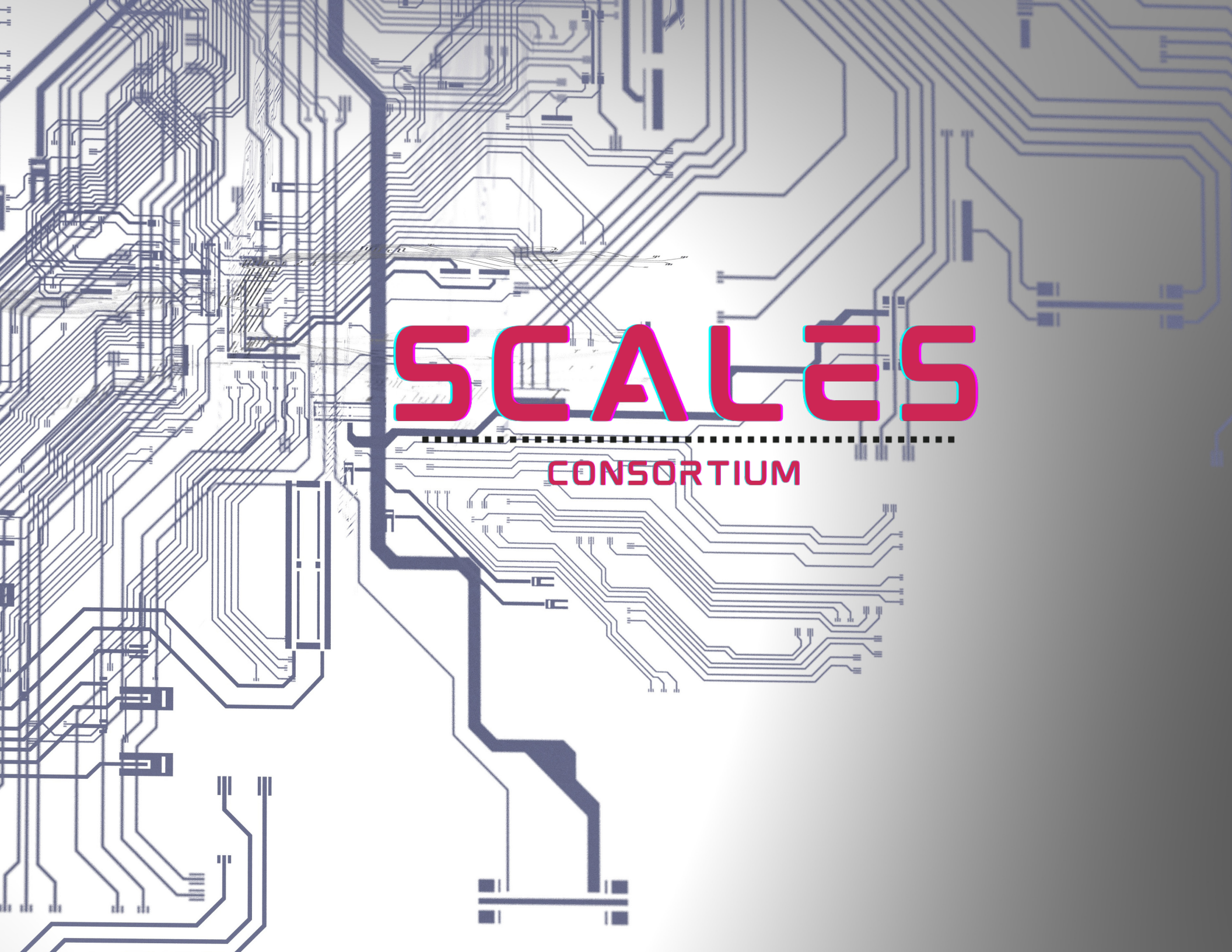

SCALES
CONSORTIUM

Contents

SCALES: Southeastern Consortium for Assured Leading-Edge Semiconductors

The Revolution Begins

When Jack Kilby, a young, new-hire engineer at Texas Instruments, and Robert Noyce—one of the "traitorous eight" who left the Shockley Semiconductor Company in 1957 to found Fairchild Semiconductor—virtually simultaneously invented the integrated circuit in the 1958 timeframe, there is no way either of them could have imagined the future tsunami of technology disruption and boundless innovation they had unleashed.

Semiconductors are the foundation for virtually every disruptive technology you can imagine; but perhaps even more impressive, they are vital to almost every aspect of our daily lives, even the most mundane. Take a moment and imagine a world in which every semiconductor suddenly disappears. Every mode of transportation would come to a grinding halt, our ability to communicate by any mode would disappear. Lifesaving medical equipment would suddenly fail. Kitchen appliances would become useless "bricks," and, perhaps most terrifying of all, you would most likely have to make it through your days without coffee!

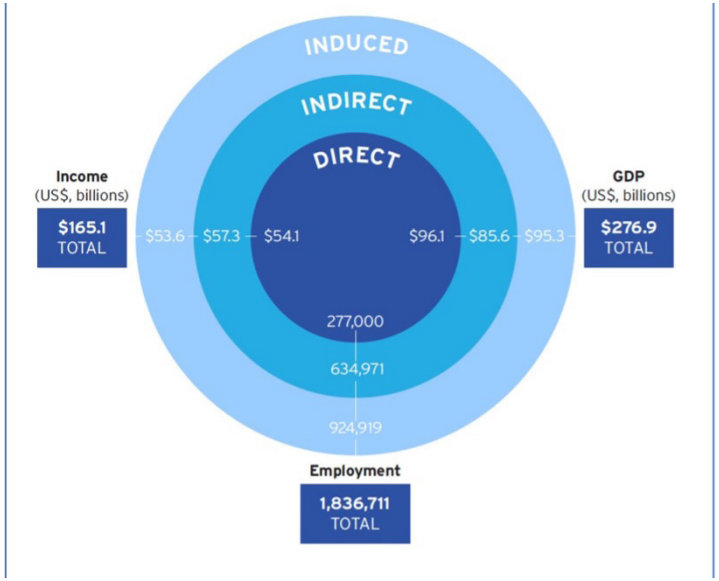
All of these basic things that we take for granted would disappear, let alone the promise of truly disruptive technologies like artificial intelligence, personalized medicine, developing advanced diagnostic and therapeutic technologies, and deploying advanced robotic systems to help our loved ones—and eventually ourselves—to "age in place" safely and with dignity.

Tremendous Economic Impact

Semiconductors are also vitally important to the U.S. economy. According to recent data

from the Semiconductor Industry Association, published in their November 2022 “State of the Industry Report”:

> *The U.S. semiconductor industry is essential to the U.S., generating value for the economy, stimulating jobs, and paying income to workers. In total, the U.S. semiconductor industry supported 1.84 million U.S. jobs in 2021. The industry directly employs more than 277,000 domestic workers in R&D, design, and manufacturing activities, among others. In addition, for each U.S. worker directly employed by the semiconductor industry, an additional 5.7 jobs are supported in the wider U.S. economy, either in the supply chains of the semiconductor industry or through the wage spending of those employed by the firms themselves of their supply chains. (See Figure below)*



Semiconductors: A Pillar of National Security and Defense

Virtually all major U.S. defense systems and platforms rely on semiconductors for their performance. If we are to outperform our peer and near-peer competitors, we must turn to smaller, more agile weapons—especially unmanned aerial vehicles and robotic ground systems—that lend themselves more readily to distributed, multi-domain operations.

As with the evolution of information technology, the concentration of computational power in an ever-smaller footprint and advances in networking will drive the development of these small systems. But in this case, the rise of artificial intelligence and the ability to conduct autonomous operations regardless of GPS availability, will also play a decisive role.

- The advantages of these smaller systems are straightforward.
- They are more resilient because they are distributed.
- They are more attritable because they are less costly and more numerous than larger assets.
- Adversaries can destroy multiple units without significantly degrading force capacity.

Losing Ground

While the U.S. has maintained a leadership position in terms of advanced semiconductor R&D, we have not fared as well in terms of retaining leading-edge chip manufacturing onshore.

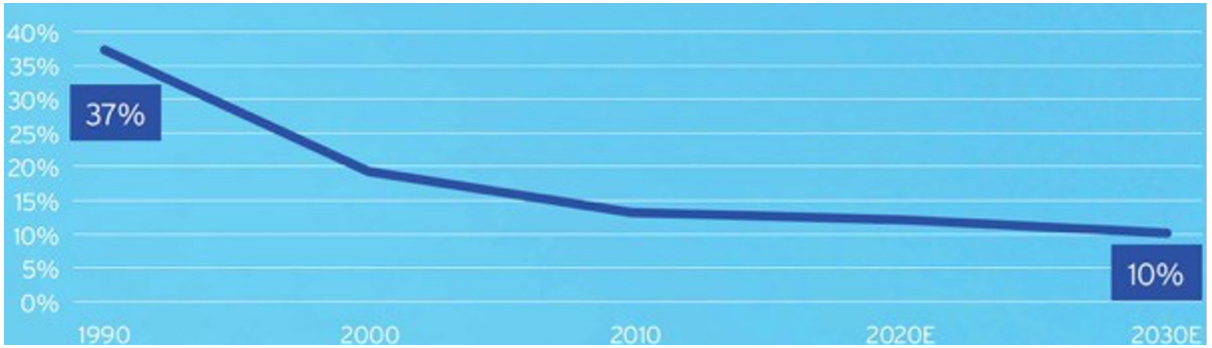
The Semiconductor Industry Association recently reported that the share of modern semiconductor manufacturing capacity located in the U.S. has eroded from 37% in 1990 to 12% today. (See Figure 2). This is mostly because other countries' governments have invested ambitiously in chip manufacturing incentives, but the U.S. government has not.

Meanwhile, federal investments in chip research have held flat as a share of GDP, while other countries have significantly ramped up research investments (see Figure 2 below).

The U.S. Government Responds

The Creating Helpful Incentives to Produce Semiconductors and Science Act of 2022 (CHIPS Act), signed into law on August 9, 2022, is designed to boost US competitiveness, innovation, and national security. The law aims to catalyze investments in domestic semiconductor manufacturing capacity. It also seeks to jump-start R&D and commercialization of leading-edge technologies, such as quantum computing, AI, clean energy, and

Figure 2

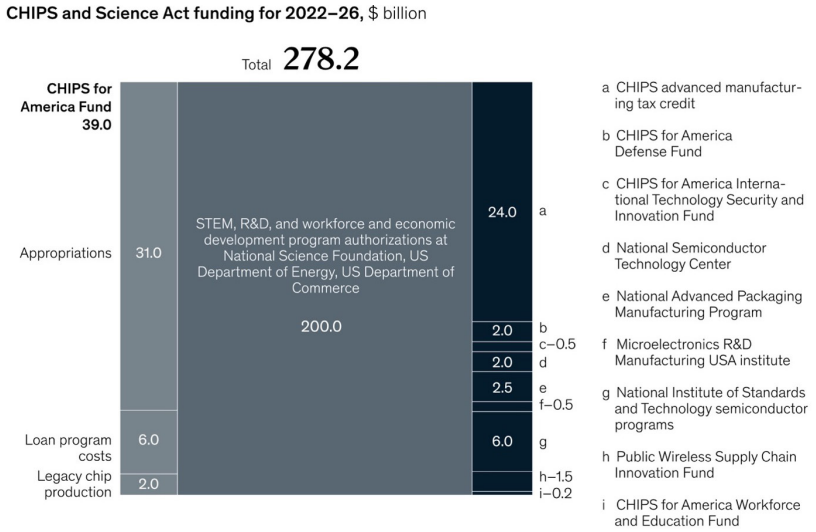


nanotechnology, and create new regional high-tech hubs and a bigger, more inclusive science, technology, engineering, and math (STEM) workforce. A breakdown is below.

The Southeast Rises to the Challenge

SCALES, the Southeastern Consortium for Assured Leading-Edge Semiconductors, was launched in September of 2022 to respond to the challenges faced by the U.S. semiconductor industry and to play a leadership role in executing the objectives set forth in the CHIPS and Science Act of 2022.

As a not-for-profit consortium of leading universities, industry members, government labs



and institutes, SCALES has built a collaborative team of the brightest minds and leading institutions to help the U.S. regain leadership across the semiconductor supply chain, from advanced R&D to manufacturing—including re-shoring critical elements of the supply chain that migrated offshore (primarily to Asia) decades ago. While SCALES's mission is intensely focused on developing clusters of manufacturing leadership in the Southeast region of the U.S., membership in the consortium is not geographically restricted. At the time of going to press, SCALES's members numbered more than sixty, including entities from as far as the Pacific Northwest, and with new members joining nearly every day.

Membership in the consortium is available at no cost. Membership will be tiered based on the engagement level of individual organizations, with a model that will include funding competitively selected upper-tier members through subcontracting instruments to execute essential research projects.

SCALES will seek funding from the CHIPS Act for an R&D center that will focus on the problems in advanced and assured packaging, integration, and merging technologies and will be organized along Thrust Areas that will be defined by the member participants. Thrusts are envisioned to span the continuum from game-changing EDA tools and methods for the design and verification, and test of next-generation Systems-in-Packages (SiPs), the development and characterization of novel materials, and reliability and assurance of leading-edge semiconductors and SiPs.

Beyond Moore's Law

The scientist and author Arthur C. Clarke once said that "Any sufficiently advanced technology is indistinguishable from magic." Although not widely published at the time, Clarke first penned this observation in 1962, only four years after the invention of the first integrated circuit.

In 1965, while working at Fairchild Semiconductor, a chemist named Gordon Moore observed that when he extrapolated computing power and cost over time, compute power increased exponentially while cost decreased at the same rate. This observation ultimately became

known as Moore's Law, and it's difficult to imagine a technology that is a better, more tangible example of being so advanced that it cannot be distinguished from magic.

But in a 2003 paper, Gordon Moore acknowledged that "No Exponential is Forever, but Forever can be Delayed." At SCALES, our fundamental belief—in fact the very foundation on which we have built our consortium—is that forever can indeed be delayed, but not by evolutionarily adhering to the strategies that kept the magic alive for more than sixty years. The dramatically transformative innovation can continue, but it will come from revolutionary disruption—disruption in the technologies and manufacturing approaches that are literally at the opposite end of the semiconductor design and fabrication process from the transistor.

The SCALES vision is that future leadership in the semiconductor industry will come from technologies like advanced packaging, heterogeneous integration, 2.5D and 3D stacking and integration, combined with novel technologies like chiplets, will be the key to continuing the staggering advancements on all fronts: compute performance, power consumption, and security, all made possible by a highly trained workforce employed in high-paying, intellectually stimulating jobs.

The Nobel Laureate physicist Richard Feynman once gave a lecture titled "There's Plenty of Room at the Bottom," in which he made the argument that the benefits of miniaturization were vast. His observation was as prescient as it was precisely correct. At SCALES, we are committed to the notion that there is also plenty of room at the top: there is almost boundless opportunity for disruptive innovation and decades of technological advancement well above the transistor level, by bringing new thinking and innovation to technologies such as Advanced Packaging, Heterogeneous Integration, novel materials, and fully exploiting the potential of innovations such as chiplets.

SCALES will execute its objectives across seven Thrust Areas that have been chosen by the organization's members and leadership. The details of our strategy and technical approaches can be found in the following pages of this document. With multiple, pre-approved, "shovel-ready" sites available in the Southeast, SCALES is poised to transform the region into a global hub of semiconductor research, development, and manufacturing dominance.

Thrust 1: EDA for Chiplets, Advance Packaging and Heterogeneous Integration (AP-HI)

The Challenge

A number of challenges prevent a successful semiconductor manufacturing industry from flourishing in the Southeast (SE) region of U.S.

- A perception that the Southeast has no major centers of semiconductor infrastructure has discouraged private investment, government funding, manufacturing locations, R&D centers, venture capital (VC) infrastructure, etc. despite the wealth of locally available intellectual skills and fundamental research activities on semiconductor technology.
- Long-held perception that, with a few exceptions, a lack of STEM-associated focus leading to less than satisfactory ranking in much needed workforce development skillsets in math and science

Historical challenges?

- Primary center of semiconductor infrastructure has traditionally been the San Francisco Bay Area, Northwest, Northeast, Arizona, and Texas
- Silicon Valley branded
- Company headquarters
- Manufacturing equipment companies and technology
- Venture capital

- Universities
- R&D, consortia, end equipment companies, etc.

Better utilization of capabilities throughout the U.S. is emerging, e.g., Austin, TX; Albany, NY; Phoenix, AZ; Dallas, TX, etc. but intellectual and physical resources in the SE are still under-utilized or continue to migrate to the major centers

Political challenges?

- Federal funding of major semiconductor centers of excellence has favored locations outside the Southeast
- Overcoming political influence of major states (e.g., California, New York, Texas) that overwhelms influence of SE states
- No strong political support in Washington, DC

Why has activity moved to other regions or countries?

- Traditionally, inability to find, hire and keep skilled resources (although this has changed dramatically in recent years as the U.S. population shifts to the SE for affordability housing, quality of life/education, climate, state tax policy, etc.
- Lack of existing semiconductor infrastructure to build upon
- Lack of well-established pathways to translate research results into practice

Why SCALES? Why the Southeast?

- Outstanding universities with leading edge semiconductor, materials and cybersecurity research, especially device assurance and advanced materials
- Mecca for U.S. Space Program resurgence and collateral electronics technologies
- Favored region for migration of populations from California and New York due to lower

cost of living, better quality of life, lower taxes, better climate, etc.

- Strong concentration of leading companies in the defense and aerospace industry
- Availability of resident talent, even though some re-training is required, especially, with veterans, and other segments of population.

Why or How are SCALES members uniquely qualified to help overcome the challenges?

- Leading semiconductor and semiconductor manufacturing equipment companies joined SCALES to take advantage of investment opportunities in the SE
- Universities with “best in class” research programs in semiconductor component assurance, new materials, etc.
- Commitment of state, county, and local Communities to invest and create microelectronic resources for the U.S. industry
- Advantageous state-driven environments for semiconductor companies to locate in SE

What are the potential growth areas?

- Advanced packaging and heterogeneous integration
- Emerging devices and systems
- Semiconductor component assurance
- EDA tooling including simulation and emulation engines
- IP creation (both hardware & software) for diverse applications (AI, ML, Analytics, etc.)

What facilities, resources (human or otherwise) can be brought to bear to overcome the challenges in the previous slide?

Partnerships between leading universities and semiconductor companies including: the University of Florida, Auburn University, Clemson University, the University of Central Florida, the University of New Orleans, Duke University, the University of South Alabama, the University of South Alabama at Huntsville, North Carolina State University, the University of North Carolina at Charlotte, the University of Arkansas, etc. Also, partnerships with Synopsys, TI, SkyWater, QORVO, Ansys, Cadence Design, CISCO, etc.

What potential advantages does SCALES have?

- World leading research programs in semiconductor component assurance, advance packaging/HI and emerging devices and systems through partnerships between universities and industry
- Partnerships between universities and leading defense and aerospace companies
- Untapped workforce development talent that includes many under-represented segments of society including veterans, displaced workers, etc.

The Action Plan

Advanced packaging and heterogeneous integration (AP-HI) of semiconductors in 2.5D or 3D chips will essentially require an electronic design automation (EDA) tool ecosystem for automatic design space exploration, optimization, analysis, & verification. Thrust 1 of SCALES will focus on developing a complete EDA tool flow for AP-HI with open-source cloud-based infrastructure. Emerging trends in 2.5D/3D electronic design bring in host of new challenges that necessitate ground-breaking innovations in automation technologies, as shown in Fig. 1 (left). The open-source nature of our EDA ecosystem will enable rapid adoption by relevant industry and make EDA keep pace with w/technology innovations by the research community.

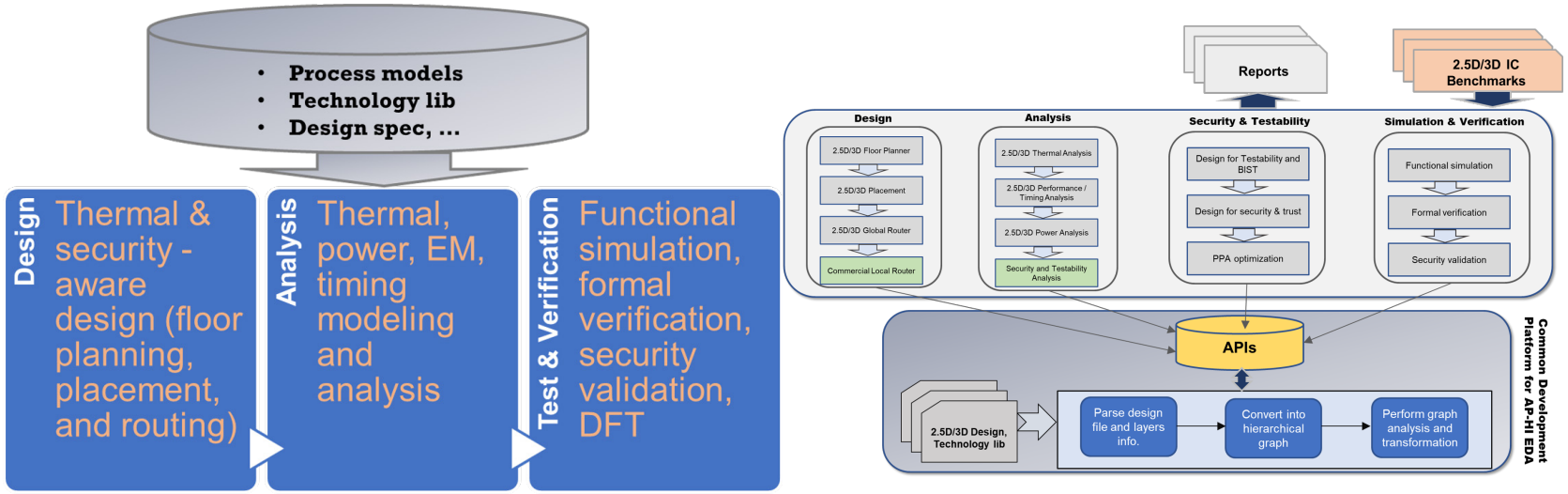


Fig. 1: Envisioned open-source EDA infrastructure for AP-HI that will interface with commercial tool offerings.

The capabilities provided by open-source EDA ecosystem will be integrated with commercial tool offerings, whenever possible, to provide complete EDA enabling of advanced multi-die chips containing logic, memory, analog, RF, MEMS, and other functions. We believe that leading-edge and affordable EDA solutions will be an essential driver for adoption and proliferation of AP-HI technologies in mid- and small-scale businesses in the southeastern region. It can drastically reduce cost, turnaround time, and complexity, provide scalability to complex designs, and minimize the need for trained specialists for harnessing AP-HI capability.

Our EDA solutions will focus on developing tools for design, with emphasis on thermal and security-aware floor planning and routing, analysis and modeling of power/temperature/EM profile and timing, and finally, simulation, verification and test. Fig. 1 (right) provides high-level view of our envisioned open-source EDA infrastructure for AP-HI. The foundation of this infrastructure will be a common development platform for EDA tools with a well-defined graph data-structure and corresponding API. All tools will be built on this foundation to improve efficiency and reliability and at the same time, to enable interoperability among the tools. Different classes of EDA tools will be developed on this framework, which can account

for the technology, process and design specifications. Such a capability can catalyze strong economic growth in the southeastern region by enabling our space, aviation, and internet of things industry with cutting-edge semiconductor design capability.

Thrust 2: Assurance (Test, Reliability, Security)

In this report we address the challenges facing assurance for advanced packaging and heterogeneous integration (AP-HI) through three angles: test, reliability and security.

TEST

Semiconductor product sizes and complexities are continuing to increase dramatically, and all of the billions of components in a device must be tested to ensure they are functional and meet the product specifications. Doing this work requires specialized skills which are becoming scarce in the US. There are several reasons for this decrease in the semiconductor test area:

- Relatively few universities in the US have an academic program which includes more than 1-2 courses in semiconductor test and related practices such as design for testability (DFT). Fewer still have labs with the associated test equipment for student use.
- Students are eschewing semiconductors and semiconductor test in favor of software and related disciplines which are more visible and popular and have higher salaries.
- In the past, the Semiconductor Research Corporation (SRC) had financed significant support for test-related research for master's and PhD students. But in recent years, those funds have been redirected to other areas and the associated faculty are moving away from test to be able to support their students. Other countries in Europe and Asia continue to fund test research.
- Semiconductor testers are expensive and are mostly located overseas where labor is cheaper. Test time availability for test engineers in the US often is not available other than overnight hours, which upsets the work-life balance and makes semiconductor test a less attractive career choice.

In short, the necessary semiconductor test education programs, skill base, and infrastructure are waning in the US which is threatening the long-term health and viability of the discipline.

RELIABILITY

With the recently introduced wafer level front-end 3DIC chip stacking technology, multiple chips/chiplets from different process technologies can be integrated "heterogeneously," such as TSMC's SoIC (System on Integrated Chips), in Chip-on-Wafer (CoW) or Wafer-on-Wafer (WoW) stackings. To make 3DIC chips even more complicated, front-end 3DIC systems can also be assembled with back-end 3DIC technologies such as Chip-on-Wafer-on-Substrate (CoWoS) or Integrated Fan-out (InFO) [ECTC '22]. Other foundries offer similar technology roadmaps [ECTC '22]. Several emerging thermal-aware design optimization techniques to mitigate thermal hotspots are needed for the new generation of 3DIC with closely-packed chiplets and strong cross-die thermal coupling. It is well understood that thermal/stress issues can severely degrade the performance and reliability of a chip and thermal runaway may occur if the temperature-dependent leakage power increases exponentially with increasing localized hotspots in a 3DIC. A large value of peak temperature and thermal gradient on-chip caused by localized hotspot and cross-die thermal coupling can have a severely negative impact on transistor performance, stress, aging, electromigration (EM), voltage drops, and timing. The following are the challenges and opportunities we can identify for the reliability area:

- Architecture-level thermal and thermal-induced stress analysis are required due to the thermal coupling from cross-die horizontally and vertically among chiplets in 3DIC. Thermal-induced stress and warpage can impact the performance of circuits such as in C4 bumps, microbumps, TSVs, extreme low-K dielectric, etc. particularly for large 3DICs.
- Modern IoT devices have extensively proliferated in various mission-critical applications, e.g., automotive, military, healthcare, industry 4.0, etc. As per ISO 26262 standard, FuSa (Functional Safety) is a technical solution to detect faults and control failures to achieve or maintain a safe state. Therefore, improving FuSa is an imperative component in the reliability sub-area of this thrust.

SECURITY

Electronic counterfeiting is a longstanding problem that has adverse long-term effects for many sectors. Untrusted parties (assembly, third-party IPs, etc.) can pirate IP (intellectual property), insert hardware Trojans, and/or include recycled, re-marked, overproduced, out-of-spec/defective, cloned, and forge-documented chips. Deploying counterfeit SiPs into security- and safety-critical systems can have severe consequences on security and reliability domains due to their sub-standard quality, poor performance, and shorter life span.

There is a significant security verification gap for HI 3DIC design, given the ever-increasing attacking surfaces and vectors from 3DIC. The most prominent gap is to have pre-silicon side-channel analysis and fault injection simulation flow in the entire silicon design procedure of HI 3DIC. We need to understand the threat models and leverage simulation tools to assess design vulnerability. Proper solutions to identify counterfeit chips before deploying them are needed, such as those making use of side channel analysis.

Why SCALES? Why the Southeast?

TEST

The southeast has excellent colleges and universities and an educated workforce. Infrastructure and land costs are inexpensive compared to locations on the west or east coasts of the US. Witness the number of worldwide automotive manufacturers that have located US manufacturing in the southeast part of the US. Despite the financial incentives to move to other topics, there are several faculty members still actively engaged in semiconductor test instruction and research at universities in the southeast, including Georgia Tech, the University of Florida, Auburn University, and others.

RELIABILITY

- SCALES members including strong academia and industry participants who could work

together complementing each other's strength to achieve a better reliability for the next generation of HI 3DIC and system reliability.

- SE partners have not only well-equipped facilities for the device/system reliability measurements such as from UF, Ansys DfR reliability facility at UMD, and reliability Q&R FA lab capabilities from Applied Material in HI-AP quick prototyping system but also have strong physics understanding and modeling/simulation capabilities.

SECURITY

Numerous universities with significant laboratories in the Southeast are well-positioned to help in this area. SCALES members have significant experience in logic locking, side-channel analysis with the use of hardware emulation, malware detection, side-channel analysis for counterfeit detection, terahertz (THz) response measurement of transistors and artificial intelligence (AI). UF has a well-equipped laboratory with photo emission equipment, among other state-of-the-art tools. Potential university partners with expertise in this area include UF, Florida International University, Wright State University, University of Texas Dallas, University of Southern Alabama (USA), and the University of Alabama Huntsville. Software vendors, such as Ansys, are actively interested in developing new tools to address pre-silicon simulation for security. This can be done in partnership with university laboratories in the Southeast to vet the simulation tools' accuracy. USA also has one of the few Riscure SCA and Fault Injection toolsets in the US and is making an investment in acquiring more tools.

Action Plan

TEST

Survey companies to identify their specific needs in semiconductor test. Formalize a pipeline of interns throughout the year to support productization of research concepts and push innovations into our products. Endow ongoing funding for graduate level semiconductor test research and to support equipment donations or purchases to teach semiconductor test to undergraduates. Incentivize semiconductor companies to create lab environments where

semiconductor test-related research can be conducted as well as production facilities for test operations. Fund the development of outreach materials that can inform middle school, high school, and college students about careers available in semiconductors and semiconductor test and the types of products they enable.

RELIABILITY

- This sub-area could study different aspects of reliability, both theoretically and experimentally, bringing together partners from industry and academia.
- First we could identify the challenges for HI 3DIC packaging as illustrated in the first section. Given the unique strengths of SE academia and industry partners, we could propose the potential projects that will provide the needed technology ensuring the leadership of HI 3DIC and Chip-Package-System reliability at US.
- Industry can help provide devices for measurement and practical expertise while academia/industry can help elucidate the fundamental physics of reliability and also provide possible modeling and simulation tools. For example, Applied Materials can provide hybrid bonding measurement and process/material inputs while academia and EDA vendors could work on fundamental physics understanding and hybrid bonding modeling/simulation tool.
- Another area we have unique strength is on the rad-hard 3DIC measurement, on-chip sensor designs, and rad-hard modeling and simulation platform. This is particularly important for electronics and HI 3DIC in extreme environment applications.
- For system quick prototyping and early system modeling and simulation, this can be a unique capability provided by the SE members for building an exemplar system to evaluate, validate and showcase thrust's various action plans. It is a rapidly deployable reference platform for chiplet-based implementation integrated into advanced package as a Heterogeneously Integrated Advanced Package System. It allows for fast time-to-prototype. It showcases the thrust's emphasis across test, security and reliability dimensions. It will be used as a demonstration vehicle for the thrust's action plan

combined with early HI 3DIC modeling and simulation platform and more broadly as a reference platform for Customers' HI-AP design & development.

SECURITY

Initially we will begin with a literature search to sort out the basic security vulnerability of HI 3DIC system, provide several case studies to prove the vulnerability, and finally a general guideline to secure HI 3DIC system with solid verification methodology.

Electrical and physical side-channel analysis (SCA) that can capture both dynamics and statics of devices in order to develop non-invasive, robust, low-cost, and applicable to mass-volume identification of counterfeit SiPs and SiP components. We will develop novel integrated IC testing and analysis methods based on terahertz (THz) response of transistors and artificial intelligence (AI) to address the challenges in the existing approaches. Existing hardware features like hardware performance counters (HPCs) and debug hardware will be used to detect malware.

Advanced Materials (AMAT) will develop an exemplar system as an overarching driving vehicle for the thrust. It will be used to evaluate, validate and showcase thrust's various action plans. It is a rapidly deployable reference platform for chiplet-based implementation integrated into advanced Package as a Heterogeneously Integrated Advanced Package System. It allows for fast time-to-prototype. It showcases the thrust's emphasis across test, security and reliability dimensions. It will be used as a demonstration vehicle for the thrust's action plan and more broadly as a reference platform for customers' HI-AP design & development.

Thrust 3: Novel Materials

The overarching challenges that Thrust 3 (novel materials) faces, and likely other thrusts face as well, is the lack of a domestic semiconductor manufacturing ecosystem in the southeast (SE) region. A healthy semiconductor manufacturing ecosystem would require vibrant research and development (R&D) programs featuring a strong industry-academia partnership, and attractive and innovative workforce development system that holistically covers all stages in the entire workforce development pipeline (from K-12 students to Ph.D. degree scientists and engineers).

Historically, despite the abundance of land, water, population, and excellent potential for manufacturing industry, the SE region has been largely under-invested in manufacturing, especially in semiconductor manufacturing that has mostly been in southwest, Silicon Valley, and some upper New York state regions. The SE region, particularly Florida, has mostly been viewed as a state for agriculture, entertainment and tourism, and real estate. However, this does not properly or proportionately represent the natural assets, technical expertise, educated populations, and potential of job growing in the SE region. In fact, the SE region has tremendous resources for manufacturing and especially semiconductor manufacturing. It has numerous growing and booming industry sectors, especially in space and defense industries. Regarding semiconductor manufacturing and high-tech industry sectors, in particular, in the SE region and Florida, knowledgeable populations have been growing, and there are many initiatives, from the state government to various organizations in many counties and cities, in encouraging the growth of high-tech companies and industries in the SE region.

Why SCALES? Why the Southeast?

The SE region is uniquely positioned for growing the Thrust 3 efforts on novel materials that will be critical for enabling the future domestic manufacturing infrastructure for heterogeneous integration (HI).

Specifically, for Thrust 3 (Novel Materials) in SCALES, the SE region has very strong technology foundation and nationally leading edge universities and industries to help develop the semiconductor industry in this region. SkyWater Technology has committed to do HI manufacturing at their Kissimmee, FL facility which will focus on the following platforms: (1) Hybrid bonding, where further scaling down in size is required and there are a lot of important materials challenges to be addressed; (2) Fan-out wafer-level packaging (FOWLP); and (3) Si-interposers. These three are currently the mainstream technologies for HI platforms, driven strongly by the defense industry base (DIB). To address the future and growing needs of DIB, SCALES Thrust 3 can integrate university-industry R&D and workforce development, and play significant roles in advancing the frontiers of the above 3 platforms.

In Thrust 3 university-industry R&D and workforce development, SkyWater, BRIDG, Synposys, and several other industry leaders all have strong presence in the SE region, and have been making great progress in developing partnerships with research universities in the SE region, including but not limited to, University of Florida (UF), University of Central Florida (UCF), Florida International University (FIU), Florida State University (FSU), University of Arkansas (UArk), Vanderbilt University (VU), Duke University, etc., along with government research labs.

In novel materials R&D, education, and workforce development, the SE region also has unique strengths in advanced semiconductors including wide-bandgap SiC and GaN and ultrawide-bandgap Ga2O3 and diamond, narrow-bandgap crystals SiGe and SiGeSn, piezoelectric and ferroelectric materials, magnetic materials (e.g., MagLab facilities), atomic layer 2D materials, quantum materials, and metamaterials. Many of these materials will play important roles in the 3 HI platforms.

To realize the envisioned advances in the key platforms and processes, and to enable the university-industry R&D and workforce development partnership, important materials growth and processing facilities need to be made available for university researchers and students.

The Action Plan

SCALES will be a leading force to create a domestic semiconductor manufacturing ecosystem in the SE region, with a unique focus on heterogeneous integration and advanced packaging. This effort will help to advance the development of the next generation of semiconductor devices and systems, and to timely address the onshore manufacturing need for the DIB and commercial customers.

In Thrust 3, SCALES members in both academia and industry will actively develop collaborative themes and projects to form sustainable partnership, in which joint R&D and workforce development can grow.

In terms of R&D, ideally the industry partners shall inform the SCALES member university researchers about the technical challenges that are awaiting innovative solutions, including in materials, processes, devices, integration, and packaging aspects. With NDA agreements for both parties, the university researchers will work with the industry partners to carry on the co-defined R&D projects. In the era of CHIPS act, the joint R&D teams will actively pursue funding and projects from all the relevant funding agencies. Overall, all these activities shall enable the creation of an HI ecosystem based in the U.S.

Workforce development will be pursued along with R&D projects with this university-industry partnership. SCALES industry members will actively provide the information on the needs of various types of workforce and requirements of technical expertise to the SCALES universities. In Thrust 3, we will focus on skillsets in fundamentals, materials growth and characterization, processes, and designs and modeling of devices that exploit unique properties of the relevant materials. Courses, certificate programs, and research topics will be developed for a whole range of students, for associate, BSE, MS, and PhD degrees.

Thrust 4: Innovative Integration and Fabrication Processing for AP-HI

Challenges

Historically, the Southeast (SE) region of the U.S. has been based on agriculture and hospitality and not much on manufacturing. To respond to the urgent needs for enhancing national security and economic interests, politicians, academic and industrial leaders realize the need to develop the semiconductor industry in this region. The U.S. semiconductor industry has dramatically lost market share over the past 3 decades for semiconductor fabs from 37% in 1990 to 12% in 2022 [PCAST 2022 report]. For advanced packaging (AP), North America's share of the global market is only 3% [Lapedus, Semiconductor Engineering 2022]. This slip in the domestic semiconductor supply chain has impacted both the defense industry base (DIB) and commercial customer economic activity. A particular concern is that DIB customers need a domestic supplier for AP solutions. Currently, these critical AP technologies reside offshore, which has a major impact on DIB customers' ability to develop vital semiconductor solutions for the U.S. Department of Defense (DoD). The DoD urgently needs state-of-the-art AP technologies to meet their current and future applications. Thus, one of the foci of SE efforts should be to develop a domestic, trusted, pure-play and open-access AP ecosystem.

From the technical perspective, with the increasing demand for the high-speed computation and broadband communication technologies in the modern hyper-connectivity society, the operation/carrier frequencies of the electronic systems are pushed up to higher microwave frequency bands including millimeter wave frequencies. For example, the fifth generation (5G) communication allocates its operation frequency to 28 GHz, 35 GHz, and 60 GHz in addition to the sub 6 GHz bands. Further, it is expected that the next generation i.e., 6G communications may use 100 GHz or higher frequencies to meet the bandwidth requirement of the future society. In the high frequency regime, there are multiple technical

challenges. One of major issues is high electrical loss and large power consumption, noise, and heat. Especially, as the frequency increases, the electrical current flows in the outermost layer of the conductor, which is called the skin effect. This causes an increase in radio frequency (RF) resistance as the operating frequency goes up, becoming a major power consuming source. Meanwhile, there are huge efforts to enhance the signal/power integrity and system performance by integrating heterogeneous chiplets into a three-dimensional (3D) fashion, i.e., 3D Heterogeneous Integration (3D-HI), which is believed to be the fourth innovation wave in semiconductor manufacturing technology [DARPA ERI 3.0]. This 3D-HI architecture, however, especially with high frequency regime, tends to produce huge heat flux issues, resulting in system performance degradation or failure. From the innovative integration and advanced electronic packaging perspective, we urgently need solutions for energy efficient interconnect, fan-out wafer-level packaging (FOWLP), interposer, bonding, and soldering technologies, their manufacturing processes, and active thermal management devices/systems. These will be Thrust 4's focus.

Why SCALES and Southeast?

The regional importance of the Southeast region includes (1) its intellectual and technical leadership in the advanced interconnect technology, and (2) the current deficiency of manufacturing infrastructure in the regional area which prevents timely translation of the technology to the society. The Thrust 4 team led by UF, SkyWater, and BRIDG helps translate the developed innovative technologies to products and startups and realize economic growth and job creation with the help of team members in the 10+ southeast states region. We plan to form a solid team for workforce development in the semiconductor manufacturing (Thrust 6 elaborates details). This will be enhanced by strong partnerships among regional governments, public, and private sectors including universities, which includes industrial profit and non-profit members. The impacts of the SCALES Thrust 4 include (1) the scientific and technical advancement in the semiconductor interconnect, thermal management, and reliability technologies, (2) the acceleration of the emergence of a growth cluster in semiconductor research, development, and manufacturing in SE, (3) the contribution to the resurgence of the nation's economic security, (4) the mitigation of socio-

economic inequities in the region, and (5) the translation of innovation into inclusive growth for broad prosperity of the community.

From a technical perspective, SCALES Thrust 4 offers a unique solution for energy efficient interconnects such as metaconductor, high density through substrate vias, bonding, and soldering. Thrust members have a strong track record in the research, have reported the highest performance metaconductor based transmission lines, inductors, and antennas to the professional societies, currently leading the field in the world. Also, thrust members offer expertise in unique transmission line architectures, thermal management technology, and well-established manufacturing processes in advanced packaging by southeast industry sectors including SkyWater, BRIDG, Micross, and i3 Microsystems.

Action Plan

Florida is rapidly growing and needs to prepare its economy for future growth. One notable success in this area is Osceola county. The county has partnered with BRIDG and Skywater Technology to develop a critical component of the semiconductor industry—AP/HI—creating NeoCity, in Kissimmee, FL. It plans to leverage its recent awarded BBBRC award, whose theme is well-aligned with that of SCALES. Future CHIPS funding requires manufacturers to partner with universities to do the necessary research and develop the future workforce in the semiconductor industry. Industry needs to develop a strong partnership with the universities in the southeastern region of the U.S., starting with the premier universities in Florida, Georgia, Alabama, South Carolina, North Carolina, Mississippi, Tennessee, Arkansas, Missouri, Louisiana, and Texas.

From a technical prospective, efforts for the innovative integration and fabrication processes can be viewed from the reduction of heat generation by adopting new interconnect materials, the development of manufacturing processes, and the development of integrable active cooling and reliability.

We plan to exploit the material for the semiconductor interconnects to perform advanced interconnect research and development, translating developed interconnect materials to

commercial usages for the modern high speed, high-signal-integrity, 3D-HI electronics applications. So a new meta-interconnect for high speed computation and broadband communication system application is demonstrated and scaled up to wafer scale (8” and 12 “ wafers) and panel scale (12” and 24”).

High efficiency thermoelectric-based active cooling is designed, implemented, and characterized. Its integrability and wafer level cooling efficiency is demonstrated.

An exemplar system for 3D-HI such as an RF transceiver module, an integrated optics module, and a wireless IoT sensing module etc. Activities will be performed in a strong partnership among industry, university, and government agencies to establish a state-of-the-art on-shoring manufacturing facilities for innovative integration and fabrication processes in the Southeast region and technical leadership in the 3D-HI field.

Thrust Five: Emerging Technologies

Emerging technologies in semiconductors and package fabrication are currently being developed in the Southeast by the region's universities and startup companies. However, until now, they have not realized their commercialization potential due to a lack of public investment. We have identified the following areas that require public investment:

- State-of-the-art (SOA) micro/nanofabrication equipment and facilities
- Micro/nanofabrication workforce training at the community college, undergraduate, graduate, and postgraduate levels
- R&D funds directed toward product development and commercialization

In Southeast universities, micro/nanofabrication training challenges exist due to a lack of access to SOA equipment. Furthermore, even if the equipment is available, there is a fear that it may break during hands-on training. For similar reasons, shared nanotech and specialized equipment with industry are not encouraged, preventing an ecosystem that would enable emerging technologies from flourishing and reaching commercialization. Additionally, the lack of R&D funds directed toward product development causes a "valley of death" scenario for commercializing emerging technologies. Historical challenges with private investors and local politicians exist in the southeast due to focusing on non-tech areas such as oil and gas, real estate, tourism, and commercial fishing. Private investment needs to be cultivated through an ecosystem of shared resources, access to a qualified workforce, and matching government funds directed toward commercializing emerging technologies.

We have also found that retention of emerging technologies and expertise is lost to other geographical areas. Students in the Southeast move to other locations to find work in semiconductor technology hubs. Professors and subject matter experts in emerging technologies are drawn away for personal financial reasons, but often are looking for

environments where emerging technologies can thrive. To retain talent in the southeast, targeted public investment in education, equipment, and commercialization of emerging technologies is needed. The investment must be designed to have a synergistic effect between startups, large corporations, academia, private investors, and local politicians.

Despite these challenges, many organizations in the Southeast region are turning to new and emerging semiconductor technologies. In academia, they promote their research, upgrade their facilities, enhance their education and training, and improve recruitment; in industry, they strengthen customer loyalty, enhance their products and services, protect market share, and win new business. In the past several weeks, we coordinated with more than 10 organizations both in academia and industry to collect the following 10 topics which belong to emerging technologies in semiconductors. The proposers have unique expertise for them. SCALES has potential advantages to support them, which will greatly benefit the southeastern region and even the nation.

Topic: Tritium Micropower Chips and Packaging

Dr. Peter Cabauy, City Labs, Inc. Miami, Florida

City Labs, Inc. designs, develops, and manufactures tritium betavoltaic micropower sources for microelectronics, sensors, and other devices commonly used in aerospace/defense, medical implants, and industrial markets. City Labs has a regulatory-licensed R&D/manufacturing facility located in Miami, Florida. SCALES can help support City Labs' goal of self-powered chips that can operate autonomously for decades without battery replacement. This will bring new classes of IoT devices, medical implants, space satellites, and terrestrial sensors. City Labs is developing semiconductor devices and packaging that incorporate tritium, a radioisotope of hydrogen commonly found in luminescent watches and exit signs. These autonomously powered tritium chips and advanced packaging will enable security and tamper prevention. The microelectronic packaging of tritium employs advanced 3D chip stacking, ultra-thin semiconductors, and designed package hermeticity to increase power output in betavoltaics. Dr. Cabauy has two decades of experience and is

one of the leaders in the tritium betavoltaic semiconductor field.

Topic: Next-generation AI and Cryptography Computing Paradigms based on Emerging Memory and Process-in-Memory (PIM) Technologies

Dr. Yiran Chen, ECE Department, Duke University

The recent research revealed that besides data storage, emerging memories can be also integrated with some novel logic circuits to perform "processing-in-memory (PIM)" – a new computing paradigm that can perform the computation of the data in-situ the memory cells and eliminate the costly data movement in conventional von Neuman architecture. PIM have been proved to have great potential in new applications such as AI computing and cryptography. The SCALES funding will help us to study design methodologies of PIM-based architecture based on emerging memories to unleash the potentials of the next-generation AI and Cryptography computing paradigms using post-CMOS technologies, offer unprecedented performance and computing efficiency.

Topic: Monolithic 3D Integrated Circuits for Data-Intensive Applications

Dr. Biswajit Ray, ECE Department, University of Alabama in Huntsville

The 3D NAND flash memory technology is an example of monolithic 3D integration which is commercially available with 232 vertical layers of floating-gate transistors. However, several challenges exist in extending the monolithic 3D integration for logic circuit design. The SCALES funding will help us to investigate the fundamental fabrication and reliability challenges associated with monolithic 3D integration technology. Commercial-off-the-shelf 3D NAND flash memory chips will be utilized as a test vehicle to explore the performance/reliability challenges with monolithic 3D integration. Dr. Ray has five years of industry experience on monolithic 3D NAND technology development and he has established a research laboratory at UAH on radiation reliability exploration of 3D NAND flash technology.

Topic: Emerging Hardware Design of Artificial Intelligence on Chip

Dr. Kasem Khalil, ECE Department, University of Mississippi

Hardware implementation of Artificial Intelligence (AI) on-chip is a hot topic of research. Such hardware, known as hardware accelerator or AI accelerator, is expected to provide as high accuracy with high speed as possible while consuming a reasonable amount of power and on-chip area. One of the research challenges is to design such hardware using less area to minimize the cost of on-chip implementation. A high-performance and low-cost AI accelerator is useful for the Internet of Things (IoT)-based applications involving security, medical and healthcare, and face recognition. The funding of SCALES will help to investigate and develop new hardware designs of AI on chip. We will establish novel optimized models and test them using a simulation tool for validation. These models will be applied to ASIC design to provide the AI model on-chip after considering the desired hardware cost and performance. This research will be connected to industry, academia, and education for advanced designs.

Topic: Emerging Hardware Security Design for The Internet of Things

Dr. Kasem Khalil, ECE Department, University of Mississippi

Hardware security is a broad term that describes the use of each hardware component to guarantee the security properties at all stages of the IC supply chain, starting from the silicon semiconductor, design, Specification, and outsourcing ICs to the after-life cycle of an IC. The goal is to design a hardware security approach with low-cost and high-security performance to be suitable for an IoT environment. The funding of SCALES will help to investigate and develop new hardware security designs. We will establish novel methods starting from semiconductor to circuit design, and these designs will mainly be based on the fabrication process. This research will be connected to industry, academia, and education.

Topic: Emerging Ink-less Additive Nanomanufacturing and Multimaterial Printing Technology for Heterogeneous Integration of Electronics and Functional Devices

Dr. Masoud Mahjouri-Samani, ECE Department, Auburn University

Additively manufactured electronics (AME) are rising as potential candidates that can enable the 2D, 2.5, and 3D integration of various functionalities, including ICs, energy harvesting, energy storage, sensors, and antennas into a single package, specifically for IoT applications. However, the current printing technologies are ink-based, which suffer from the complexity of ink formulation, limited printing materials, and ink-associated contaminations. We have recently pioneered a novel additive nanomanufacturing and dry multimaterial printing technology to integrate various functional materials and devices on flexible and rigid substrates. The SCALES funding can help us further advance this emerging technology and thoroughly investigate its fundamental science and engineering aspects. In the long run, with SCALES support, we will establish the first multimaterial and heterogeneous printing platform with a focus on research, education, and workforce development to serve academia, industry, and defense sectors.

Topic: Multifunction Devices and 3D Platform for Enhanced Spectrum and Thermal Efficiency

Dr. Guoan Wang, Department of Electrical Engineering, University of South Carolina

High frequency devices and circuits with multiple functionalities and frequency reconfigurability enabled with novel thin films (e.g., ferroelectric and ferromagnetic), advanced microfabrication techniques and additive manufacturing methods are designed and optimized to enable efficient spectrum utilization for wireless communications and high-performance computing applications. New 3-Dimensional thermal dissipation platform is developed with 3D printed devices providing efficient thermal dissipation efficiency, interference mitigation and electromagnetic functionalities Dr. Wang has over

20 years industrial and academia experiences in the field with more than 140 publications in journals and peer-reviewed conference proceedings, 53 granted US and international patents, and 51 US patents pending. SCALES can enhance and expedite the technology development and commercialization with the advanced facilities and the network-centric collaboration platform.

Topic: Radio Frequency Detection and Identification of Single Cells

Dr. Pingshan Wang, ECE Department, Clemson University

Dr. P. Wang works on devices, circuits, and systems for high-throughput, radio-frequency (RF) spectroscopic detection and identification of single biological cells as well as electron spin resonance spectroscopy. In addition to nanofabrication, MEMS devices, heterogeneous packaging, and CMOS RFICs, quantum microwaves, RF interaction and control of biological microorganisms, and automotive electronics are also part of his research area.

Topic: Novel Semiconductor Device

Dr. Nezih Pala, ECE Department, Florida International University

Faculty in FIU has experience in wide bandgap materials and devices (III-N, diamond etc.), high-bandwidth terahertz (THz) communication for on-chip and inter-chip (let) wireless interconnects, RF-microwave-millimeter wave devices and systems, nanophotonics and plasmonics for optical interconnects and optical quantum computing, microbatteries and micro fuel cells for on-chip power supply.

Topic: Emerging Device Enabled Secure and Reliable Storage and AI System

Dr. Jinhui Wang, ECE Department, University of South Alabama

Emerging devices (such as various memristors) and relevant non-ideal characteristics, physical theories of semiconductor device (such as Fowler-Nordheim tunneling mechanism), and cybersecurity models (such as differential privacy) are utilized and

optimized to enable secure and reliable storage and AI system for computing and critical applications. Dr. Wang has worked on this topic over 15 years and taped out microchips for memristors, 3D IC, 2.5D IC, AI accelerator, processor, mixed-signal IC, as well as published 160+ related papers in leading journals and conferences. Currently, SCALES can help upgrade the facilities and equipment for more complex and small feature size emerging device fabrication and characterization. In the long run, SCALES can help and support to integrate all resources in Southeast and build up public platform to serve industry, academia, and education for advanced semiconductor emerging technologies.

Emerging technologies in semiconductors and advanced packaging will bridge the gap, facilitate growth, and prepare future leadership in academia and industry in the Southeast region by the following actions:

In Academia

1) Most of the facilities and equipment in academic organizations are micro scale or sub-micro scale, so, academic organizations will collaborate with SCALES to equip the advanced technology and package facilities for the emerging semiconductor device design and manufacture. 2) Development of the emerging technologies needs interdisciplinary expertise, qualified engineers and workers need training from physics, material science, electrical engineering, computer engineering, computer science, and even system engineering, academic organizations will collaborate with SCALES to build cross-department training program. 3) Because of NDAs (Non-Disclosure Agreements) or other legal agreements and export control restrictions, sometimes academic organizations need a long time to negotiate and sign an NDA and manufacture chips and devices from commercial foundry. With SCALES, academic organizations may have further collaboration with the foundry to shorten such process.

In Industry

1) Industries in the Southeast will collaborate with SCALES by providing internships and employing nanofabrication and advanced packaging workers trained at partner academic institutions. 2) Shared cleanroom facilities with state-of-the-art micro/nanofabrication equipment and facilities will be utilized and supported by industry. An ecosystem of cutting-edge equipment and facilities throughout the SCALES region will enable workforce retention and spur emerging technologies and startups in the Southeast. Additionally, it will attract corporate facilities, private equity, and venture capital investment for emerging technologies in the Southeast. 3) Commercialization of emerging technologies will be achieved through SCALES funding to be matched by private investment. SCALES product development funding will be utilized to combat the “Valley of Death” scenario for emerging technologies.

Thrust 6: Workforce Development

The Challenge

Anticipated growth in the domestic semiconductor-chip manufacturing ecosystem is currently challenged by workforce-development barriers. Beyond the chip manufacturers, this ecosystem includes equipment and service providers that support manufacturing (e.g., design services, technology computer-aided design software providers, materials, manufacturing and characterization equipment vendors, heterogeneous-integration and packaging, testing and qualification industries, etc.), and customers that use semiconductor chip products to produce highly functional components, sub-systems, and systems (i.e., the rest of the microelectronics industry). Without appropriate regional investments throughout the various sectors and levels of the value chain associated with the microelectronics industry, these workforce-development challenges will only increase. Below is a short list of these challenges identified through meetings with representative from SCALES industrial partners:

- There is a mismatch between the demand for new employees (i.e., technicians through Ph.D.) and the ability of American colleges and universities to produce them.
- This situation is exacerbated by the fact that the semiconductor industry has an aging workforce and is anticipating the loss of many of their most knowledgeable and experienced employees.
- The future workforce, in particular Gen-Z, has been surrounded by a cyber environment since childhood, which builds an interest toward those careers.

Although the south-east region of the US (i.e., from Louisiana and Arkansas on the west, to Florida through North Carolina on the east) has a small percentage of the national semiconductor-chip manufacturing capability, it provides a higher percentage of the equipment manufacturers and national packaging infrastructure. The fact that the southeast

region boasts a growing population, a considerable number of large public community colleges and universities (e.g., >25% of the top 20 public universities), and low personal and business taxes provides real opportunities for the growth and/or relocation of advanced microelectronics companies to this area. However, companies in this region have struggled (especially recently) to meet their employment needs. Hiring out-of-state talent often presents retention challenges due to the lack of familial anchors and the high compensation packages offered by employers located in very-high-cost states (e.g., California, etc.). The matriculation of regional talent into 2-year community college through Ph.D. programs is not adequate in the specific topics needed by the national semiconductor industry as a whole and the southeast region in particular.

In the past, community colleges in Florida (e.g. Valencia College) and North Carolina (e.g., Central Carolina Community College) had established two-year Associate of Science (AS) and Associate of Arts (AA) degrees in the semiconductor space to serve their local industries. However, past off-shoring of the semiconductor industry has led to a lack of growth in semiconductor jobs and eventually the mothballing of these community college level programs. There exists a tremendous opportunity to reestablish these programs and to re-shape them in ways that specifically support the new and evolving needs of the local industry.

Resources and Opportunities

Government and industry have invested considerably in the southeast region over the past decade. There is a tremendous talent pool in the region considering that three of the top five largest schools in the US (UCF, UF, and FIU each having more than 50,000 students) and some of the highest nationally ranked engineering programs (Georgia Tech, UF, NCSU) are located in this region. In addition, there is a huge population of minorities and veterans in the southeast providing the perfect grounds for a sustainable and diverse highly-skilled workforce. Some of the recent synergistic developments and facts in southeast region are including but not limited to:

- The partnership between Skywater Technologies and BRIDGE as one of the main public/private partnerships for semiconductor device fabrication
- University of Florida Preeminence program to hire top 500 faculty across the nation
- University of Central Florida's strategic investment in hiring 20 new faculty in the area of semiconductor and the establishment of a new semiconductor manufacturing degree program in partnership with Valencia College.
- New acquisitions and development plans by regional companies such as Micross, Renesas, Qorvo, Wolfspeed, I3 electronics, etc. to hire hundreds of employees in Florida
- Strong presence of defense industrial business such as Lockheed Martin, Northrop Grumman, Raytheon, L3Harris, Radiance Technologies, Dynetics, in Florida, Alabama, etc.
- Presence of equipment vendors such as Plasmatherm and Trion (in Florida) and ClassOne Equipment (in Georgia)
- State-level incentives for small businesses and startup-up fabs to take advantage of the government funding and establish new facilities in the region

Action Plan

The SCALES Workforce Development Team, which consists of members from universities and colleges as well as industry across many sectors and parts of the value chain, has a plan to develop a sustainable, scalable, and distributed infrastructure to provide a regional source of well-trained individuals (pre-college to Ph.D.) that are capable of meeting the immediate and future needs of the semiconductor industry.

Pre-College

- At this first stage of the workforce development pipeline, our focus is on engaging with the K12 population to raise awareness of well-paying and rewarding technical careers in the semiconductor industry.

- Activities will include visits to industry facilities, tours, and meetings with junior engineers, and a discussion of future career opportunities, training requirements, and ranges of compensation.
- In addition, “gamification” of microelectronics education will be utilized as a means to drive greater career engagement and awareness.

Community College

- Training related to the microelectronics industry will be restored where previously existing and added where new. In all cases the programs will be well tailored to the needs of the industry located in the broader community of the college.
- Modernize the educational plans to meet the evolving interests of Gen-Z and industry
- Upskill workers from other industries, including military veterans
- Reduce barriers to educational pathway (e.g., scholarships, some participant-support costs, etc.), and provide paid internships to train technicians

University

- Shared facilities and resources in the southeast region among universities, community colleges, and startups to help build skilled cohorts
- Leverage digital twins and virtual reality capability to scale up access and knowledge
- Paid internships to train undergraduate engineering students with guaranteed jobs post internship
- Paid hands-on training of students in on-campus co-op programs integrated with the existing university cleanroom facility operations on campus
- Faculty industrial summer internship at industrial partner sites to learn the latest industry needs and trends.

In order to successfully execute the proposed plans listed above, the rough order of magnitude budget request made by this thrust is $75M+ over 5 years.

Thrust 7: Investment, Commercialization, and Demonstrators

The Challenges

Investment and Capital Generation

There is a perception that the Southeast region has no major center of semiconductor infrastructure. This view has historically cut across the supply chain, and applies to capital equipment manufacturers, materials suppliers and fabs. This "image problem" has discouraged private investment, government funding, manufacturing locations, R&D centers, venture capital (VC) infrastructure, etc., despite the wealth of intellectual skills available locally, and the existence of clusters of exceptionally strong centers of excellence in universities, commercial industry, government laboratories and research institutes.

While not unique to the Southeast, investing in hardware and capital intensive companies—especially at the startup stage—is inherently risky, and, over time, VCs and private equity investors have turned their focus to lower-risk investment opportunities, most notably software and "app" companies where the up-front investment and risk of failure are seen as lower, and the potential "carry" is more assured.

Historical Geographical and Ecosystem Challenges

The San Francisco Bay Area has historically been recognized as the center of semiconductor infrastructure in the U.S. by most key measures. There is a perception that the entire U.S. semiconductor ecosystem is centered in the Bay Area.

- Company headquarters locations
- Manufacturing equipment companies and technology

- Concentration of Venture Capital firms, i.e., Sand Hill Road
- Top-tier universities including, but not limited to, Berkeley and Stanford
- R&D, consortia, end equipment companies, hybrid trade association-consortia such as SEMI
- Highly trained workforce

Political Challenges

On the political front, the Southeast has a strong U.S. delegation, but does not have a particularly strong track record of coming together to support large federal initiatives that broadly benefit the region. Moreover, the Southeast has lacked a champion who is analogous to Senator Schumer in NY, who is virtually recognized as a "pro-semiconductor brand."

And, generally speaking, the Southeast has largely been overlooked when it comes to large, federally funded initiatives such as the Manufacturing USA Institutes.

Why SCALES? Why the Southeast?

The Southeast is well-positioned with outstanding universities with leading-edge semiconductor, materials, and cybersecurity research, especially device assurance and advanced package and materials fabrication. The SCALES universities are attractors of talent, large corporate facilities, startups, and investment capital. The region is favored by migrating populations from California, New York, and the rest of the country due to the lower cost of living, the better quality of life, lower taxes, a pleasant climate, and a favorable regulatory environment. It has a strong concentration of leading aerospace and defense companies in areas such as Huntsville, Alabama and the I-4 corridor in Florida. Additionally, Miami, Florida, has become the new epicenter of investment capital firms and is continuing to grow. Bridg/SkyWater and i3 offer a nucleus for semiconductor manufacturing and advanced package fabrication and areas such as Austin, Texas continue to grow and attract semiconductor-based companies.

Action Plan: The Way Forward

The CHIPS Act of 2022 includes a major Strategic Imperative that, if the Southeast region can come together in a coordinated manner, should create significant, "first-ever" opportunities to address the challenges laid out in this document. The goal of this initiative is to catalyze private sector investments and the excerpted text follows.

> *Catalyze private sector investment. A successful CHIPS program will respond to market signals, fill market gaps and reduce investment risk to attract significant private capital. The role of government in the CHIPS program is to shift financial incentives to maximize large scale private investment in production, break-through technologies, and workers. The CHIPS program will encourage new ecosystem partnerships that reduce risk, build on U.S. strengths, and facilitate such investments.*

While the details of this particular initiative are not fully fleshed-out, and specific opportunities have not been released in the form of an RFP, one has to believe that a strong coordinated effort from the Southeast region can leverage this opportunity to great advantage.

One can envision accessing funding for capital-intensive, hardware-centric startups aimed at re-shoring key elements of the semiconductor supply chain and creating an ecosystem in the Southeast that will rival that of Austin, Albany, and even the Bay Area.

Because of the very large base of corporations in the aerospace and defense sector located in the southeast—particularly Alabama, Georgia and Florida—a teaming arrangement is planned among the defense corporations and the universities to attack specific capabilities targeted by the CHIPS Act. These include 3D heterogeneous integration utilizing leading edge foundry capability from QORVO (headquartered in North Carolina) with leading simulation and mechanical design programs at the University of Florida, University of Alabama at Huntsville and Auburn University. Coupling one of the nation-leading hardware security programs at the University of Florida with Synopsys, leading edge component assurance capability will be developed and provided in the form of design software and

hardware testing. Finally, leading edge semiconductor materials science and engineering from Clemson University, the University of South Carolina and the University of Florida will be teamed with the world's leading suppliers Silicon Carbide in North Carolina and emerging new ones in South Carolina.

Additionally, SCALES will leverage new, U.S. Government-backed VC-like sources of funding including, but not limited to, the DoD's Trusted Capital Program and the Office of Strategic Capital—programs that can address the historical reluctance of traditional VC firms to invest in capital-intensive, hardware-centric startups.

While the epicenter of venture capital for semiconductor technology has traditionally been the San Francisco Bay Area, there has been a recent mass migration of investment management companies to Miami from the Northeast and Midwest. Teaming with this group of firms to finance the ongoing development and growth of leading-edge technology in the Southeastern United States offers a major opportunity for sustaining the growth of new developments.

SCALES Members

Adam Khalifa
Ahmad Chamseddine
Alan Mantooth
Ali Mohammod
Ant Ural
Avik Ghosh
Baibhab Chatterjee
Baoyun Ge
Beau Bakken
Ben Larry
Biswajit Ray
Bo Ren
Cathy Lee
Charles Hages
Chris Ferekides
Christophe Bobda
Chuck Woychick
Chunlei Wang
Daryoosh Vashaee
David Arnold
David Huitink
David Lishan
Deirde Hanford
Domenic Forte
Donna Joyce
Ebrahim Amiri
Elizabeth Unger
Erin Patrick
Eunjung Kim
Fareena Saqib
Farimah Farahmandi
Fathi Amsaad
Fisher Yu
Gary Hunt
George Clark
Gloria Kim
Goutam Koley
Greg Creech
Greg Stitt
Guoan Wang
Henry Zmuda
Honggyu Kim
Ian Getreu
Ivan Ruchkin
Jack Judy
Jason Milstein
Jay Lewis
Jeffery Allen
Jennifer Hite
Jeremy Adams
Jia Di
Jing Guo
Jinhui Wang
Joel Harley
John Allgair
John Damoulakis
Jon Mellott
Josh Caldwell
JT McDonald
Justin C. Borski
Kanad Basu
Kasem Khalil
Kathryn Cribbs
Ken Butler
Ken Merkel
Kevin Hoopingarner
Kevin S. Jones
KK Lin

Kostas Mallios

Lang Lin

Magdy Bayoumi

Mark Land

Mark Law

Markondeyaraj Pulugurtha

Martin Margala

Masoud Mahjouri Samani

Matt Francis

Md Jahidul Islam

Md Tauhidur Rahman

Mehdi Sadi

Michael Alles

Mike O'Brien

Mircea R. Stan

Mohamed Chouikha

Mohammed Shahbaz Hussain

Mona Ebrish

Monica Allen

Najme Ebrahimi

Navid Asadi

Nezih Pala

Nicholas C. Hooten

Norman Chang

Oliver Brand

Parag Bannerjee

Peter Cabauy

Peter O'Donnell

Pingshan Wang

Prabhat Mishra

Robert Sarkassian

Rashmi Jha

Reza Abdolvand

Reza Azarderakhsh

Rick Clemmer

Robert Taylor

Rockwell Hsu

Rodrigo Alvarez

Ron Schrimpf

Ryan Need

Samson Melamed

Samuel Russ

Sandip Ray

Sanghamitra Roy

Scott Thompson

Serge Leef

Seungdeog Choi

Shahram Jamshidi

Shahrokh Saeedi

Sharon Weiss

Shimeng Yu

Shiwen Mao

Shuo Wang

Soheil Salehi

Srinivas Katkoori

Stephen Pearton

Subi Kengeri

Swarup Bhunia

Tan Wong

Terry Back

Thomas Martin

Todd Andel

Tommy Morris

Tony Trinh

Toshikazu Nishida

Travis Anderson

Tung Phan

Ujjwal Guin

Wally Rhines

William Eisenstadt

Xiaoqing Song

Yarui Peng

Yiran Chen

Yong-Kyu Yoon

Youping Chen

Yousef Iskander

Yuxi Xie

Zhong Chen

SCALES Entities


UNIVERSITY OF NORTH CAROLINA
CHARLOTTE


USA
UNIVERSITY OF
SOUTH ALABAMA


UNIVERSITY OF
SOUTH CAROLINA


UNIVERSITY of
SOUTH FLORIDA


UTD
THE UNIVERSITY
OF TEXAS AT DALLAS


UNIVERSITY of VIRGINIA


STATE


VANDERBILT
UNIVERSITY


WRIGHT STATE
UNIVERSITY


ALIGARH MUSLIM
UNIVERSITY